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Possible SCD/RSE Trigger Module

Real-Time Systems Engineering Department
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Background

Wes recently mentioned that there are three candidate trigger modules for SBND (Nevis/uBooNE, Penn Trigger Board/DUNE 35-ton, and National Instruments hardware/ICARUS), and he suggested that it would be useful for those of us in Fermilab SCD to describe our PREP Modernization work that might be relevant.

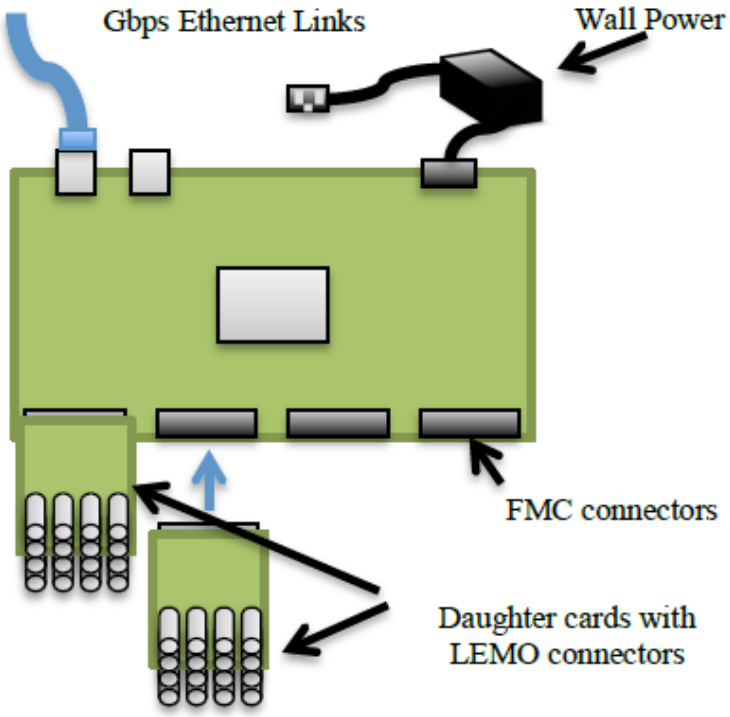
In these slides, we describe this work and how it might be modified to provide some amount of trigger functionality.

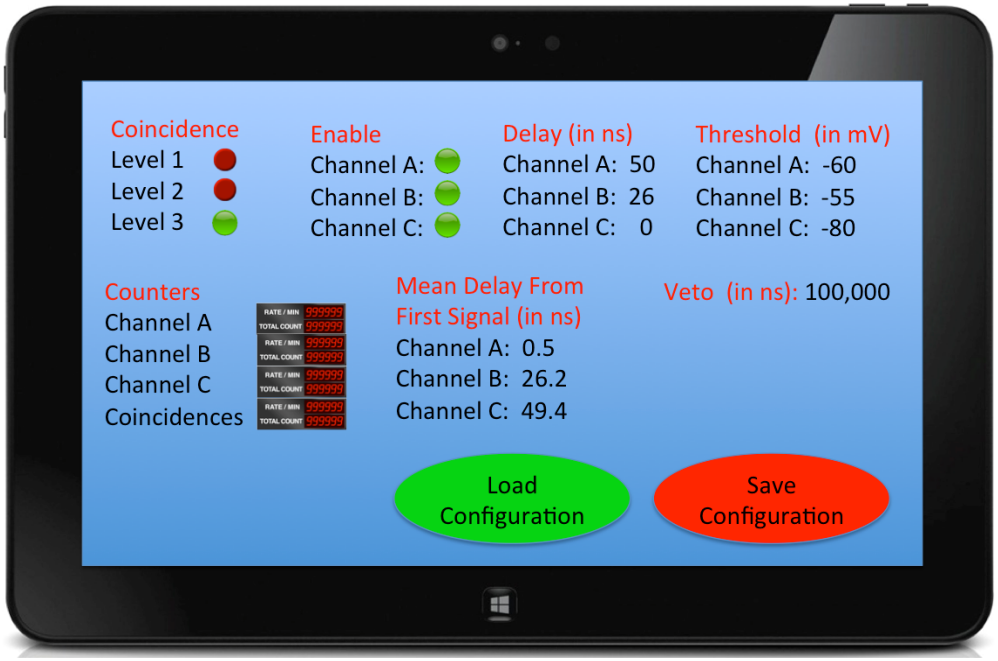
[Slide 9 was added after the meeting, and its goal is to summarize the questions and suggestions that came up.]

PREP in the FPGA Era

Vision: gradually replace aging commercial electronics with general-purpose FPGA boards and appropriate daughter cards

Initial candidate: NIM coincidence module

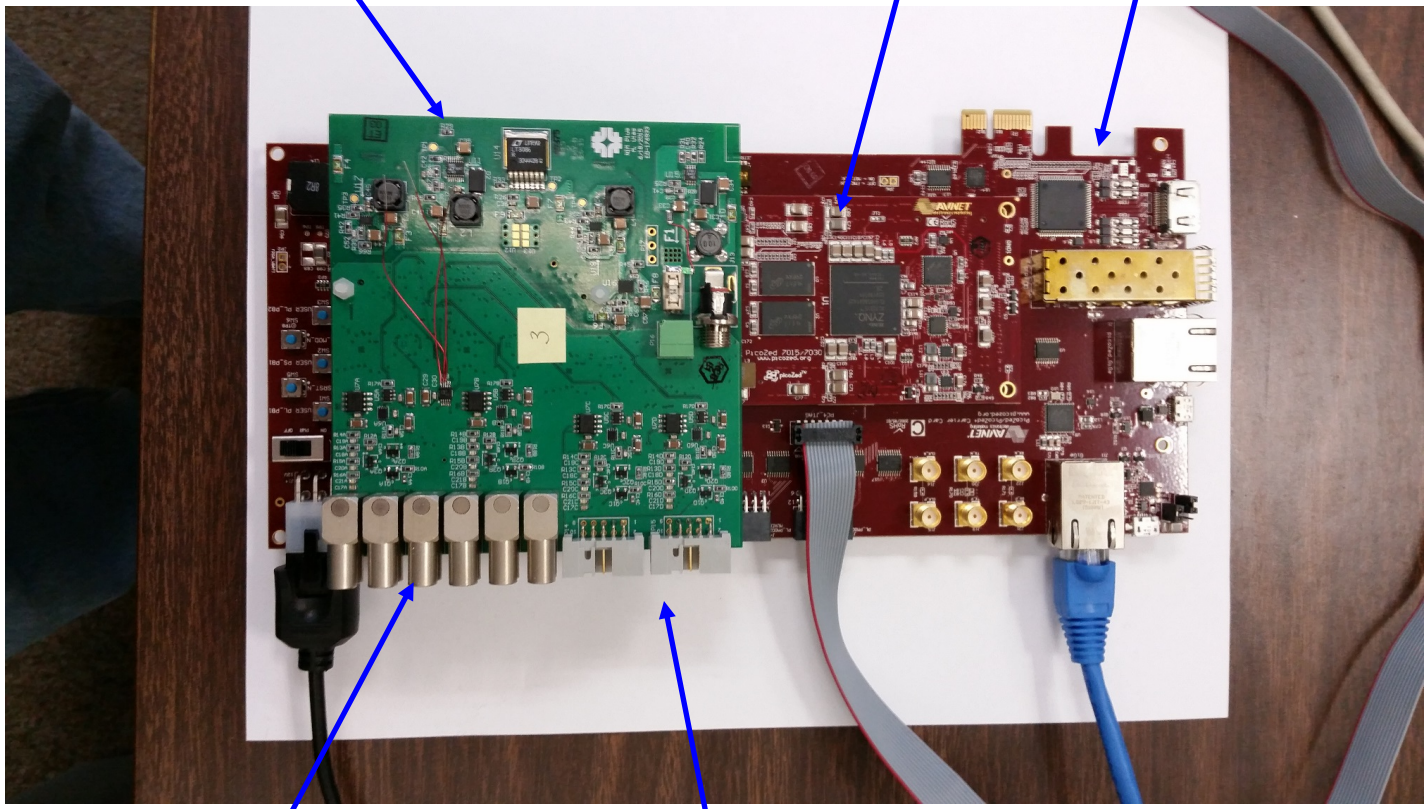




NIM Plus Board

PicoZed Board

PicoZed Carrier Board



Signal Inputs, Outputs

LVDS Inputs, Outputs

FPGA-Based NIM Coincidence Module

Hardware & Firmware

- Receive NIM or TTL or LVDS signals
- Look for coincidence of programmable number of signals
- Output signal can be delayed and/or stretched
- Internal clock provided, external may be possible
- BUSY signal

External Interface

- Web-based control and feedback

FPGA-Based NIM Trigger Module

Hardware & Firmware

- Receive NIM or TTL or LVDS signals
- Look for coincidence of programmable number of signals
- Output signal can be delayed and/or stretched
- Internal clock provided, external may be possible
- BUSY signal
- Accept INHIBIT signal to prevent generation of output signal
- Counters of input pulses, inhibit-ed output pulses, etc, etc

External Interface

- Web-based control and feedback
- Programmatic control and readout
- Readout of counters and composition of individual trigger decisions

Target Dates for Coincidence & Trigger Module Features

April 30th – development of the firmware, deployment on the PicoZed on the testbench, manual testing of all functions

June 30th – development of the web interface with control functionality, some amount of register readout, and some amount of counter readout

Later in the summer and fall:

- Programmatic interface
- Additional readout functionality (e.g. individual trigger composition)
- Diagnostic firmware and software
- Firmware and software for automated testing
- Documentation: user guide, tester guide, etc.

Longer-term – incorporation of this module into the PREP pool

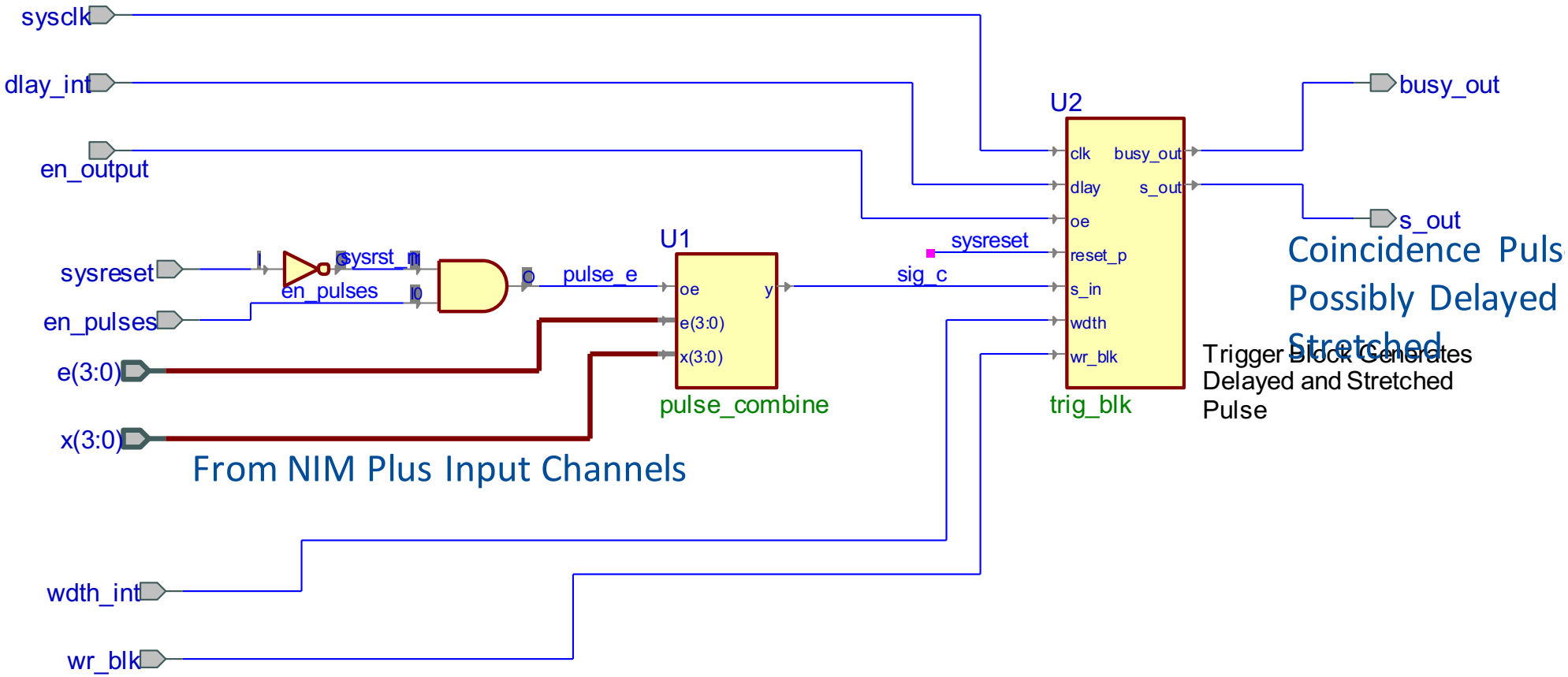
Our Understanding of the SBND Trigger Module

1. Accept some number of NIM or TTL inputs and support configurable combinations of these inputs to generate an overall trigger signal
2. Support an "inhibit" signal that suppresses the output of the overall trigger signal
3. Keep internal counters on the number of each type of input triggers that were received within a given time interval, ditto the number of output trigger signals, ditto the number of times an input signal was inhibited. Probably also the wall-clock time spent inhibited. Provide a way to periodically read out these values.
4. Support event-by-event read out of which trigger signals went into the overall trigger
5. Rate needs?
6. Double-pulse separation needed?
7. Other requirements?

Questions and Suggestions from the Meeting

1. How will calibration of input signal thresholds be handled? (to be determined)
2. Are the trigger decisions pipelined? (Initially no, but it may be possible.)
3. Stretch and/or delay input signals.
4. Prescale inputs.
5. Packaging is important: mechanical stability of connections; routing of cables in a real experiment.
6. Keep internal log of timestamps when signals are above threshold and the output is ON (for later readout and validation).
7. Multiple different output signals (trigger table).
8. Other options include the LArIAT CAEN module with firmware from Mike K. Also, the DarkSide-50 CAEN V1495 with FW from Boris B.
9. Talk more with Angela, Wes, Eric, and Georgia.

Backup Slides

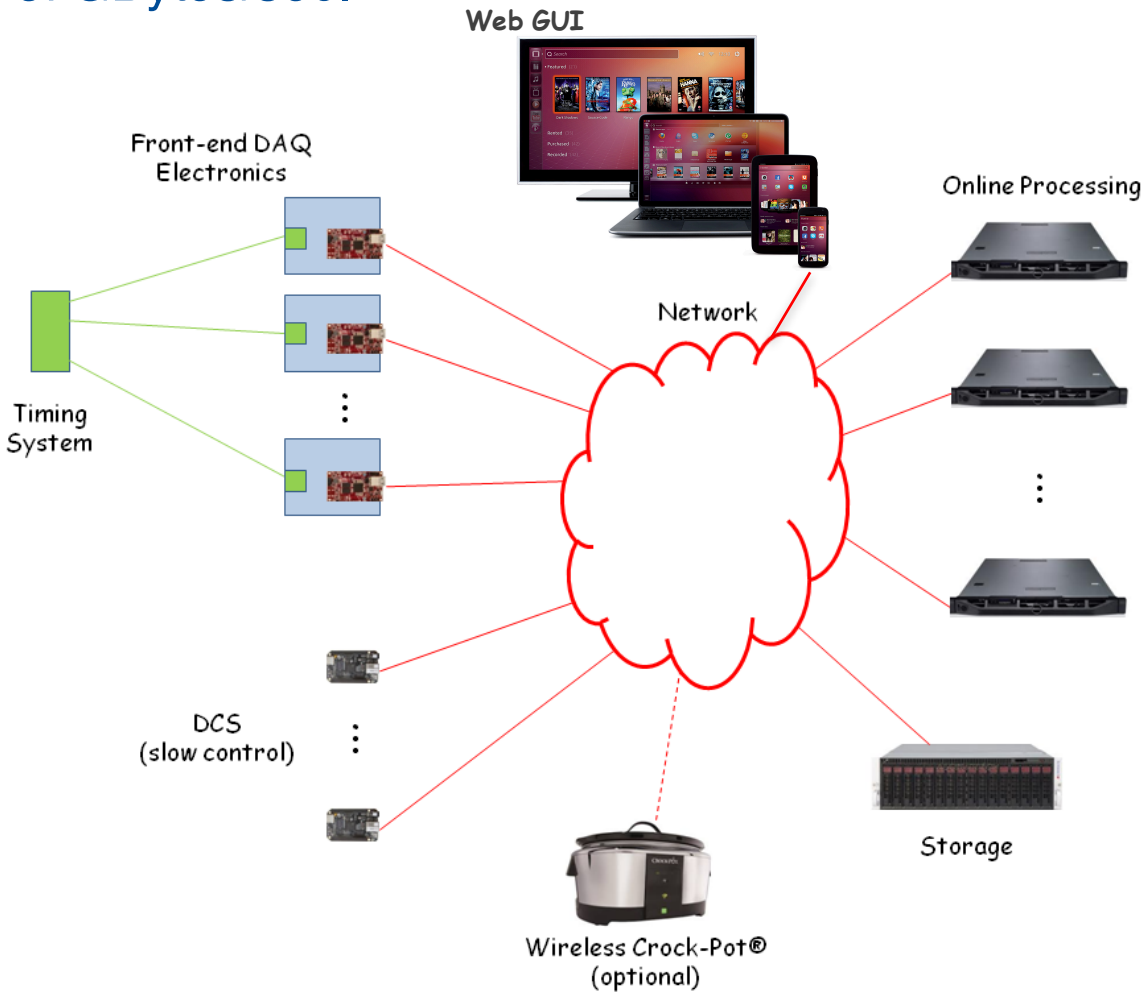

sysclk
dlay_int
en_output
sysreset
en_pulses
e(3:0)
x(3:0)
From NIM Plus Input Channels
wdth_int
wr_blk
I
sysrst_n
en_pulses
I0
O
pulse_e
U1
oe
y
e(3:0)
x(3:0)
pulse_combine
sysreset
sig_c
U2
clk
busy_out
dlay
s_out
oe
reset_p
s_in
wdth
wr_blk
trig_blk
busy_out
s_out
Coincidence Puls
Possibly Delayed
Stretched
Trigger Block Generates
Delayed and Stretched
Pulse

Off-the-Shelf DAQ LDRD

- 2 years of effort for OtS DAQ **proof-of-concept**:
  - Survey the market for candidate IoT boards.
  - Focus on 1 board in each range (Low, Mid, and High) to populate initial menu.
  - Develop a JavaScript GUI for control and readout using web browser.
  - Develop host and embedded APIs for socket based communicated between *artdaq* and candidate boards.
  - Develop sample reusable firmware components.
  - Test and catalog available features and supported data rates.

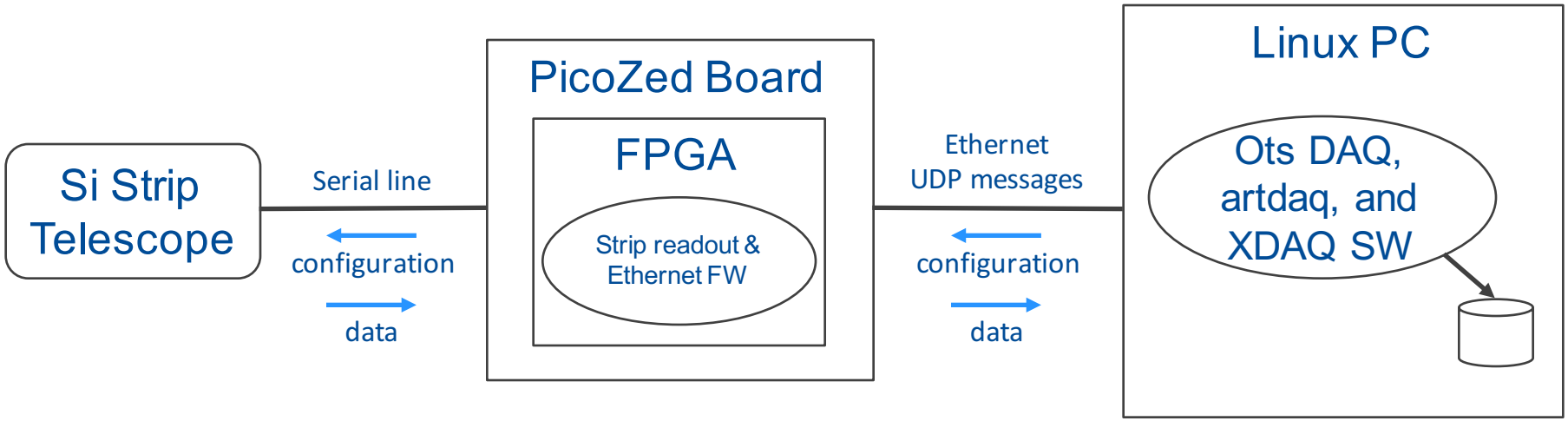
Off-the-Shelf DAQ Model

- We are developing a **low cost**, data acquisition architecture **as a service**, based on commercial **IoT** technology that is **scalable** from a few MBytes/sec to hundreds of GBytes/sec.

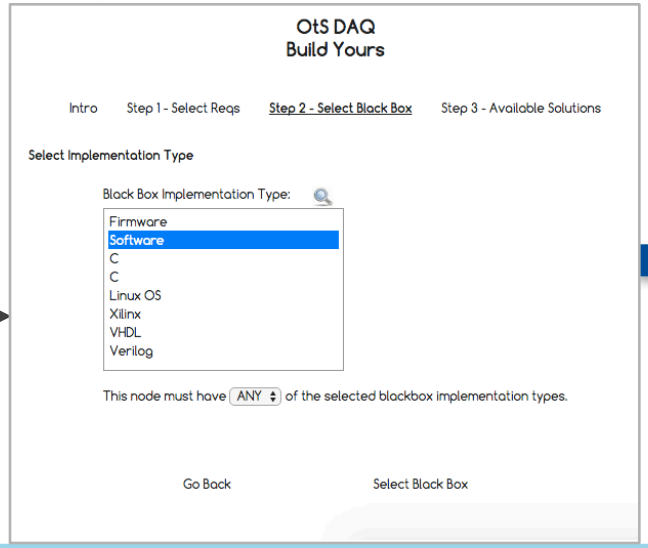


Off-the-Shelf DAQ - Status

Demonstration of detector readout (at FTBF)



Development of the OtS DAQ web site



To: User
Subject: Your OtS DAQ

Tar files can be downloaded from here:
Location of FW: URL1
Location of SW: URL2